**Explain why the following memory modules are used:**

|  |  |
| --- | --- |
| HDD | Less costly  Can store more  Storage memory is secondary memory, requiring cheap and non-volatile storage device. Data center frequently involves data exchange, therefore, NOR flash and NAND flash are not suitable with certain W/R lifecycle. HDD is cheap and has nearly infinite W/R times, which is suitable for storage memory. |
| SDD | More costly  Stores less  More robust  Limited W/R cycles  Memory array based on NAND-FLASH or NOR-FLASH.  Various techniques used to extend the life of SSD  –Wear levelling is a technique used to extend the life of the SSD disk by distributing data erase/write operations evenly over the entire disk.  –Use External RAM as buffer to minimize the number of writes to Flash in SSD.  –Error Correction Code. Ability to recover from one or more bits of error in media. |
| NAND | Given the features of the memory: robust, large capacity and non-volatile.  EEPROM(roughly a few megabytes) and NOR flash(roughly 64MB to 2GB)do not satisfy large capacity as they are around few megabytes.  NAND is more robust to movement compared to HDD.  ----------------------------------------------------------------------------------------- |
| NOR |  |
| EEPROM | SRAM, DRAM should be out as they are volatile memory. A common mistake for this question is that student may choose flash memory.  However, they ignore an important signal: Each set data is < 64 bytes and can be erased without affecting other sets of user configuration. This means the erase block size is < 64B. Flash memory has an erase block size ~4KB, which is way larger than required size. EEPROM has an erase block size ~16B, which is suitable.  ----------------------------------------------------------------------------------------- |
| DRAM  volatile | DRAM Read Process destroys information stored on capacitor  The process of measuring charges on a capacitor also effectively discharged it i.e. data is destroyed.  Hence, the original data has to be re-written back after every read.  Periodic refresh is needed as the stored charge “leaks” with time.  The basic DRAM is more or less obsolete in the market today. It is replaced by its synchronous version called Synchronous DRAM (SDRAM).  –Periodic refresh required.  –Small (1 to 3 transistors per cell).  –Slower.  –Higher power consumption due to need for periodic refresh operation to maintain data integrity of memory cells. |
| SRAM  volatile | Static Random Access Memory  –Data stored as long as supply is applied.  –Large (4 to 6 transistors per cell).  –Fast.  –Low power consumption (active and standby) |

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**Serial vs parallel**

1. Less issue with signal skew and less probability of being influenced by crosstalk.

2. Less bulky so easier to route PCB trace and cabling.

3. Modern serial standards can achieve relatively high data transfer speed even though data is transferred one bit at a time. USB replacing Parallel Port Interface, SATA replacing IDE

Parallel: Fast data transfer rate (more bits can be transferred at one time)–Hardware interface design tend to be simpler as only strobe signals are needed.

Affected by Signal Skew and Cross Talk, which limits the maximum clocking speed and transfer distance. Hardware (data cable) can be bulky if data width is large. Need more space to route the PCB traces. Higher hardware cost compared to Serial data implementation.

Serial:

Less affected by signal skew and crosstalk because there are less electrical wires involved compared to parallel data transfer. Hence, able to support higher frequency clocking. Able to transfer data reliably over a longer distance. Lower cost since less wires and connectors are needed.

Data transfer rate lower given the same clock rate since only one data line is available. Hardware interface design typically more complex as it need to handle serial to parallel conversion (Processor typically only process in bytes or multiple bytes).

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**SSD can still claim high MTBF**

The following techniques are used to extend the life of SSD:1. wear levelling, which is to distribute data and erase/write cycles evenly over the entire disk2. use of external RAM as a buffer to minimise the number of writes to Flash in SSD.

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**Why eject drive if ssd is used**

If an external RAM is used as a buffer in SSD and the “Eject Drive” option is not executed before attempting to unplug the SSD, the RAM might not have enough time to store its data to Flash in SSD. This may lead to data loss since RAM is volatile in nature.

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**FIFO vs LRU**

FIFO policy replaces the block that has been in the cache the longest, regardless of when it was last used. LRU policy replaces the block that has been unused for the longest period of time.

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**Write allocate and write no allocate**

**Write through and write back**

Write Hit: Write through updates cache and main memory simultaneously on every write. Write back (also called copyback) updates memory only when the block is selected for replacement.

Write Miss: Write allocate=> fetch on write. A write miss will cause the data block at the write-miss address to be loaded to the cache. Write-no-allocate=> A write miss will not cause the data block to be loaded to the cache. Data Write is done directly to its location in main memory.

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**Cache and Internal RAM**

Cache is faster than internal RAM

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**Asynchronous vs Synchronous**

Synchronous: Transfer can be done at a higher clock rate as a clock signal is used to strobe the data signal.

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**Differential Signaling vs Single-Ended**

Using differential signal will increase the resistance of the signal, preventing from noisy environment.

Differential signals has better noise tolerance so is able to be clocked at higher frequency.

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**What is the difference between carry and overflow?**

Carry: Set when the register cannot properly represent the result as an unsigned value (no sign bit required).

Overflow: Set when the register cannot properly represent the result as a signed value (you overflowed into the sign bit)

Function:

Carry:

1.Combined with the second highest carry bit to detect overflow.

2.Use as the additional bit in order to perform addition of big number that is larger than the size of the register.

Overflow:

1.Use to detect out of range, so that wrong result can be notified.

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**Carry vs overflow**

Unsigned Numbers

–Carry = 1 always indicates an overflow (new value is too large to be stored in the given number of bits

)–The overflow flag means nothing in the context of unsigned numbers

Signed numbers

–Overflow = 1 indicates an overflow

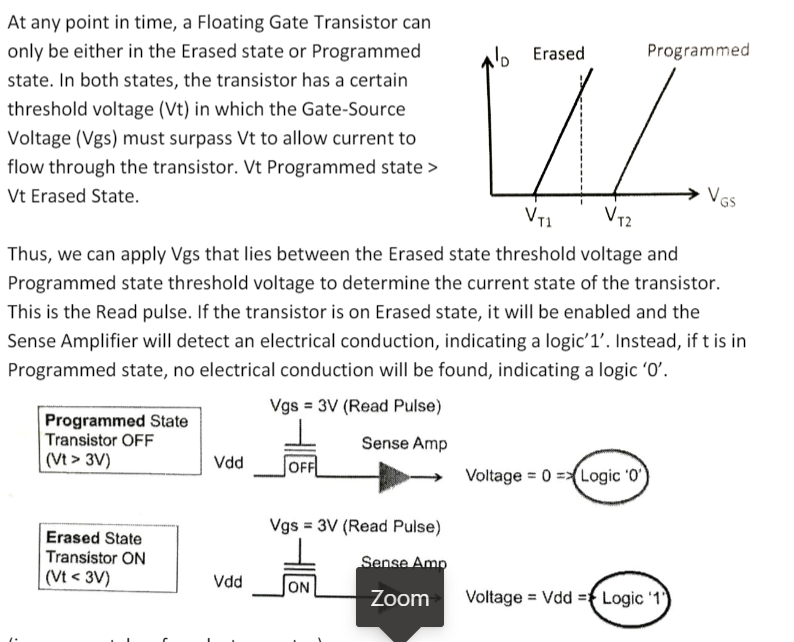
–Carry flag can be set for signed numbers, but this does not necessarily means an overflow has occurred.

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**VGT**

At any point in time, a Floating Gate Transistor can only be either in the Erased state or Programmed state. In both states, the transistor has a certain threshold voltage (Vt) in which the Gate-Source Voltage (Vgs) must surpass Vt to allow current to flow through the transistor. Vt Programmed state > Vt Erased State.

Thus, we can apply Vgs that lies between the Erased state threshold voltage and Programmed state threshold voltage to determine the current state of the transistor. This is the Read pulse. If the transistor is on Erased state, it will be enabled and the Sense Amplifier will detect an electrical conduction, indicating a logic ’1’. Instead, if t is in Programmed state, no electrical conduction will be found, indicating a logic ‘0’.



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**SPI vs UART**

SPI is a synchronous data transfer protocol while UART is asynchronous. SPI is able to transfer any number of bits in a continuous stream without any interruption. UART transfers data in packets instead, each containing a fixed number if bits, including data overhead that will interrupt the transmission. When transferring data of the same size, using UART protocol requires transferring a greater number of bits than SPI due to necessary data overhead. All this limits the maximum transfer rate that can be achieved using UART, making it significantly lower than SPI.

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**Fixed point vs floating point**

Fixed Point Representation

-Advantage: Fixed precision within the entire range of representable numbers.

-Disadvantage: As the number of bits allocated for both integers and fractional values are fixed, some of the bits may not be fully utilized when certain values are being represented.

Floating Point Representation

-Advantage: Provide a very large range of representable numbers by sacrificing precision for larger numbers

-Disadvantage: Rounding error may occur especially for computation using larger numbers

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**Criteria for storage element**

Power consumption

–Data centers consumed a lot of power, which not only translate to direct cost in utility and cooling measures, but also limit its choice of location.

–Centers are commonly found near natural cooling elements such as large natural water bodies which offer a low cost and reliable source of cooling.

Speed

–Beneficial for caching databases and other data affecting overall application or system performance.

Robustness

–Tolerance to various form of mechanical movement/interference increases reliability and reduces need and cost of maintenance.

–Drive housing structure shock absorption requirement is also reduced.

Heat production

–The less heat generated the less cooling and power required in the data center.

Size

–Data centers will be able to store more data in less space, which increases efficiency in all areas (power, cooling, etc.)

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**SRAM vs DRAM**

